IN THE CLAIMS

Please amend claim 11 to read as follows:

11. (Twice Amended) A structure of an Electrically Erasable Programmable Read-Only Memory (EEPROM), comprising:

a silicon oxide substrate having a source/drain region,

a tunnel oxide layer disposed over said silicon substrate;

a select gate disposed over said tunnel oxide layer, wherein said select gate is defined by a conductive layer covered with a first insulated material thereon and comprises a sidewall made of a second insulated material;

a sidewall forming a single floating gate aligned to one side of said select gate;

a third insulated material located directly on said tunnel oxide layer, said select gate and said floating gate; and

a control gate formed on said third insulated material.

Please renumber proposed new claim 12 added by the Preliminary Amendment filed on March 18, 2003, as new claim 16 to follow the proper sequential numbering of the claims and please amend this claim to read as follows:

~~16.~~ 15. (Amended) A structure of an Electrically Erasable Programmable Read-Only Memory (EEPROM), comprising:

a silicon substrate having a source/drain region,

a tunnel oxide layer disposed over said silicon substrate;

a select gate disposed over said tunnel oxide layer, wherein said select gate is defined by a conductive layer covered with a first insulated material thereon and comprises a sidewall made of a second insulated material;

a floating gate aligned to one side of said select gate;

a third insulated material located directly on said tunnel oxide layer, said select gate and said floating gate; and

a control gate formed on said third insulated material, wherein said control gate partially covers said third insulated material.